DESIGN AND SIMULATION OF CMOS BASED LOW VOLTAGE BANDGAP REFERENCE CIRCUITRY

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DESIGN AND SIMULATION OF CMOS BASED LOW VOLTAGE BANDGAP REFERENCE CIRCUITRY

By

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LIST OF ABBREVIATION

BGR	Bandgap Reference
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
BJT	Bipolar Junction Transistor
CMOS	Complementary Metal Oxide Semiconductor
CTAT	Complementary To Absolute Temperature
GBW	Gain Bandwidth
ICMR +	Maximum Input Common Mode Range
ICMR -	Minimum Input Common Mode Range
LDO	Low Drop Out
MOS	Metal Oxide Semiconductor
Op-Amp	Operation Amplifier
OTA	Operational Transconductance Amplifier
PDA	Personal Digital Assistant
PLL	Phase Lock Loop
PTAT	Proportional to Absolute Temperature
TC	Temperature Coefficient
V_{EB}	Voltage Base Emitter
VDD	Voltage Supply

REKABENTUK DAN SIMULASI LITAR SELA JALUR BERVOLTAN RENDAH BERDASARKAN CMOS

ABSTRAK

Kajian ini bertujuan untuk mengkaji prestasi litar sela jalur dengan menggunakan transistor semikonduktor oksida logam (MOS) bagi menggantikan litar transistor simpang dwikutub (BJT). Sebagaimana yang diketahui, BJT mempunyai ciri-ciri yang lebih baik terhadap suhu, namun begitu, BJT memerlukan voltan ambang yang lebih tinggi untuk beroperasi berbanding MOS transistor. Oleh sebab itu, BJT telah digantikan dengan MOS transistor untuk meningkatkan prestasi sela jalur bagi aplikasi voltan yang lebih rendah daripada 1.2V dan juga untuk mengurangkan proses fabrikasi. Hasil daripada Op-Amp, ia mampu mencapai gandaan sebanyak 74.34dB dan 62.16 degree pada tahap fasa margin yang mana ianya stabil bagi integrasi dengan litar sela jalur. Selepas itu, litar Op-Amp telah dimasukkan ke dalam reka bentuk sela jalur yang lengkap. Reka bentuk litar sela jalur yang dicadangkan dapat mencapai prestasi yang menghasilkan voltan rendah maksimum kira-kira 446.05mV dan minimum 440.2mV pada julat suhu -10 ℃ kepada 100 ℃. Selain itu, voltan rujukan yang dihasilkan adalah stabil selepas voltan bekalan lebih tinggi daripada 1.2V digunakan. Ini bermakna litar masih mampu untuk menyediakan voltan rujukan yang tepat dan stabil dengan pelbagai variasi perubahan bekalan voltan. Tambahan juga, litar mempunyai nilai PSRR tinggi pada -70.59 dB untuk memastikan ruang yang cukup dalam mengurangkan hasil bunyi daripada pembekalan voltan. Walau bagaimanapun, litar mempunyai pekali suhu yang lebih tinggi iaitu 118.12 ppm / ℃. Akhir sekali, reka bentuk ini telah dilengkapi dengan susun atur simulasi akhir dan kawasan litar sela jalur termasuk ‘dummy’ telah menggunakan 133μm x 140μm.

DESIGN AND SIMULATION OF CMOS BASED LOW VOLTAGE BANDGAP REFERENCE CIRCUITRY

ABSTRACT

The objective of this thesis is to study the performance of the BGR circuit by using Metal Oxide Semiconductor (MOS) transistor to replace the Bipolar Junction Transistor (BJT) circuit. As known bipolar transistor is better characterize over temperature. However, bipolar transistor required a high threshold voltage to operate as compared to MOS transistor; Therefore, the bipolar transistor has replaced by MOS transistor to improve performance of BGR for low voltage application lower than 1.2V and to reduce fabrication process. The result of the Op-Amp has shown it able to achieve 74.34dB gain as well as 62.16 degree of phase margin, which stable for integration with BGR circuit. After that, the Op-Amp circuit is then incorporate into the design of for a complete BGR architecture. The proposed design of BGR circuit able to achieve similar performance, which produce the maximum low voltage about 446.05mV and the minimum of 440.2mV at a temperature range of -10℃ to 100 ℃. Besides, the reference voltage generated is stable after the supply voltage higher than 1.2V, which meant the circuit are still able to provide accurate and stable reference voltage for a variety of supply voltage changes. Furthermore, the circuit has high PSRR values at -70.59 dB, to ensure enough headroom for noise rejection from the supply voltage. However, the circuit has a higher temperature coefficient which is 118.12 ppm /℃. Lastly, the design completed with post-layout simulation and the area of BGR circuit including dummy are being consume of 133μm x 140μm of die area.

Chapter 1

INTRODUCTION

1.0 Introduction

Voltage reference is the electronic component that provides a constant output voltage that regardless of variations in external conditions such as temperature, loading and pressure. Now, voltage reference circuit is one of the essential building blocks for many devices such as analog and mixed signal electronic devices like data converter, power management controller, oscillator, PLL, LDO, memory circuit and others.

As the process technologies is built up, the demand for low-voltage operation is getting more popular. Many circuits are design to operate at low voltage as it consumes of low power consumption. Likewise, low power consumption the rapid of increased demand on mobile electronic devices such as cellular phones, PDAs, camera recorders, and laptops also one of the factor causing low voltage are become popular [1].

In certain circumstances, it needs a voltage reference that able to handle the change of temperature. Thus, in conventional BGR design, the circuit are able to handle temperature change with small voltage variation. Therefore, when the reference voltage increases with the temperature, it is known, as proportional to absolute temperature (PTAT) voltage. On the other hand, when the reference voltage decreases with the temperature, it is known as complementary to absolute temperature (CTAT) voltage. BGR voltage reference can designed using the combinational of PTAT voltage and CTAT voltage so that the reference circuit is independent of temperature.

The research carried out in this thesis, is to design a bandgap voltage reference circuit that able to produce small output voltage that independent of temperature change.

1.1 Problem Statement

Bandgap voltage references (BGR) are widely applied in today's circuits as references with it able to provide constant output voltage with independent of temperature change. The advantage in BGR circuit make it become popular to use in many system example in measurement circuits and metering applications demand a very low temperature coefficient to maintain the desired precision over the entire temperature range, application in mobile or even in temperature sensing.

Nowadays low-voltage operation become more popular, many circuits are design to operate at low voltage as it consumes of low power consumption. IC design is now predominated by low power, low voltage objectives, making CMOS the technology of choice. A conventional bandgap reference output is about 1.24 V [1], which is almost equal to the bandgap of silicon. However, in modern deep-submicron technology, a voltage of around 1 V is preferred.

It is known that the base-emitter voltage of the bipolar transistor is better characterized over temperature and varies less than the threshold voltage and the mobility of the MOS transistors. Thus, most of the voltage references use the bipolar transistor's pn junction as the basis of reference generation [2]. However, the conventional output voltage of BGR is 1.24V, which is nearly the same voltage as the bandgap of silicon.

Besides, bipolar transistor required a high threshold voltage to operate as to compare with Metal Oxide Semiconductor (MOS) transistor. Thus, the power consumption of bipolar transistor also higher than MOS transistor. Therefore, the bipolar transistor has replaced with MOS transistors to improve performance of BGR by

generating the low voltage reference and to reduce the complexity of the fabrication process of BJT. The combination of different operating regions like subthreshold, linear and saturation of MOS suppresses the temperature dependence of voltage reference [3].

1.2 Research Objectives

The main objective of this research is to investigate and design a conventional bandgap circuit with substituting Bipolar Junction Transistor (BJT) to the MOS transistor for low voltage reference. In order to support the main objective, the following specific objectives were structured:

i. To design an Op-Amp that able to achieve $\geq 60\ dB$ gain and $\geq 60\ °$ phase margin.
ii. To design and simulate a low voltage reference with a conventional BGR circuit by substituting BJT transistor to MOS transistor.
iii. To simulate and characterize the performance of the BGR circuit.

1.3 Scope of Limitation

The aim of this research is to study and design a BGR circuit which having low voltage variations. The scope of study is confine in the following areas:

i) The circuit designed is only in Complementary Metal Oxide Semiconductor (CMOS) compatible process.

ii) Supply voltage range is 1.8V to 3.3V.

iii) The temperature range is from -10℃ to 100℃.

1.4 Thesis Structure

This dissertation divided into five chapters. In Chapter 1, which is the introduction of the dissertation, will provide a background of the research, problem statement, research objective and scope of study as well as dissertation organization.

Chapter 2 the Literature Review , which will about discuss the basic concept of BGR circuit and operation amplifier (Op-Amp) used, moreover types of BGR circuit will also be discussed in this chapter .

Chapter 3 the Methodology, this chapter explains the methodology of the proposed BGR circuit form the implementation down to completed BGR circuit with integration to Op-Amp circuitry.

Chapter 4 the Result and Discussion, this chapter present the simulation analysis, observations and detail of measured data.

Chapter 5 the Conclusion and Future Works, this chapter are the final chapter of that concentrates on the research conclusion and areas in the future of improvement.

Chapter 2

LITERATURE REVIEW

2.0 Introduction

The bandgap reference has been a popular analog circuit for many years. In 1971, Robert Widlar introduced the Op-Amp with model LM113, the first band-gap reference. It used conventional junction isolated bipolar-integrated circuit technology to make a stable low-voltage (1.220V) reference. This type of reference became popular as a stable voltage reference for low-voltage circuits. Bandgaps used in digital integrated circuits, to provide a local bias that is not adversely affect by ambient noises or transients [4].

In the past, there are two basic kinds of popular of voltage reference design Zener-based voltage reference and Bandgap voltage reference. The Zener-base voltage reference has better accurate, however it has a limitation which is it need a minimum power supply required which is at least of 6V to operate. With today's technology we needed a very low voltage supply to reduce the power consumption, thus Zener-base voltage reference are not that popular as compared to the BGR voltage reference [4].

The BGR voltage reference can designed using the combinational of with two different voltage, which is proportional to absolute temperature (PTAT), and complementary to absolute temperature (CTAT) as in Figure 2.1 so the reference voltage generated is independent of temperature. PTAT voltage has a positive temperature coefficient with generated by taking two differences in the base-emitter voltage of two bipolar transistor and CTAT voltage has a negative temperature coefficient which is generated by the voltage across base-emitter voltage. By having these two quantities as

a factor in the design it resulted the Bandgap voltage has approximately zero of temperature coefficient [4].

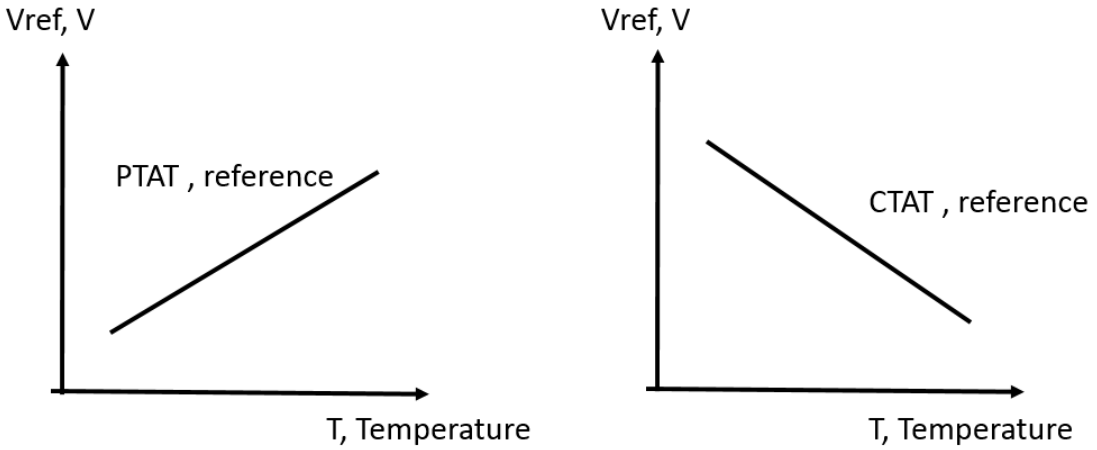

Figure 2.1 : (a) PTAT and (b) CTAT Voltage Reference [5].

This chapter present and discuss the Op-Amp circuity and different types of BGR circuit is review. As form, different authors there are different goal or design intention to achieve in each of the circuits such as temperature coefficient improvement, voltage variation reduction, extended of BGR temperature operating range etc.

2.1 Operational Amplifier

Op-Amps are widely used in electronic devices nowadays. It is also an important component found in the BGR circuit. In many applications, the gain of the single-stage amplifier is often not adequate [6]. Therefore, to achieve sufficient the most common type of Op-Amp used is two-stage Op-Amp with compensation capacitors.

Todays, there have a lot of Op-Amp topology, two stage Op-Amp is one of the Op-Amp, which normally used when the circuit need to have high gain and low output impedance.

2.1.1 Two Stage Op-Amp Circuit Review1 [6-7]

Op-Amp are the basic block of many analog circuit design as it provided better speed and high accuracy, however, this two element are depend on the bandwidth and the DC gain of the Op-Amp. The larger of the bandwidth and the gain, the better of the speed and accuracy of the amplifier.

The general block diagram of an Op-Amp with output buffer shown in Figure 2.2. This first block in the left is the differential input stage, which have two terminal input signal which one input is the positive terminal while the other input is negative terminal. It will provide the differential voltage to the amplifier circuit. The second block is the second stage of the amplifier or known as a second gain stage. This function of this circuit is to transform the differential signal to single ended signal. The output buffer stage provides the low impedance at output and larger output current need to drive the load of Op-Amp or improves the slew rate. This stage might be drop as it depends on the circuit design. When the output stage does not use the circuit is an operational transconductance amplifier (OTA). The motive of the compensation circuit is to decrease the gain at high frequencies and to maintain stability when negative feedback is apply to the Op-Amp [7].

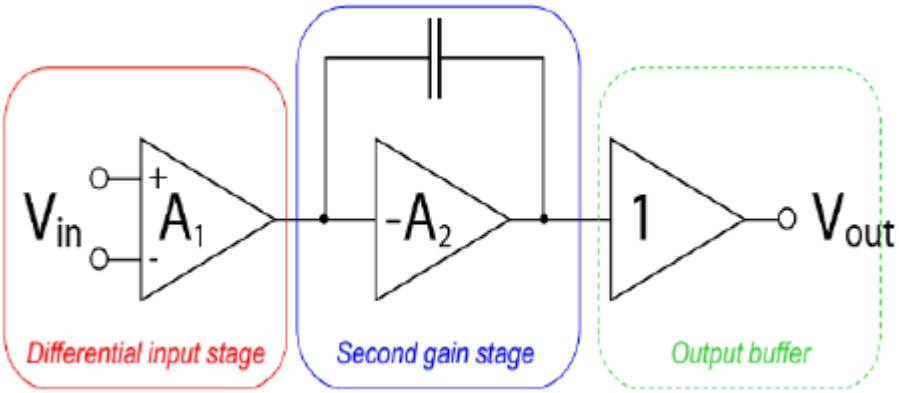

Figure 2.2: Simplified Block Diagram [7].

In general, the gain provided by the first stage of the amplifier was not sufficient, thus it needs additional amplification to achieve high gain, and this to been completed by introducing the second stage of the amplifier. Besides the gain, in real circuit implementation, it consists of the biasing circuitry. The function of the biasing circuitry is to provide the proper operation point to each transistor used in amplifier and make sure they are operating in the saturation region.

Figure 2.3 shows the classical two-stage Op-Amp configuration. Transistor M5 provides biasing for the entire amplifier while M1 and M2 form a differential pair of the input to the amplifier. [6] Transistor M5 and M7 supply the differential pair with bias current and transistor M3 and M4 form a current mirror. The second stage of the Op-Amp is formed by M6, which is a common-source amplifier actively loaded with the transistor M7 [6]. The total gain of the amplifier is the summation of the gain in the first stage and second stage. The compensation capacitor CC is to achieve the gain frequency characteristic with dominant pole [8].

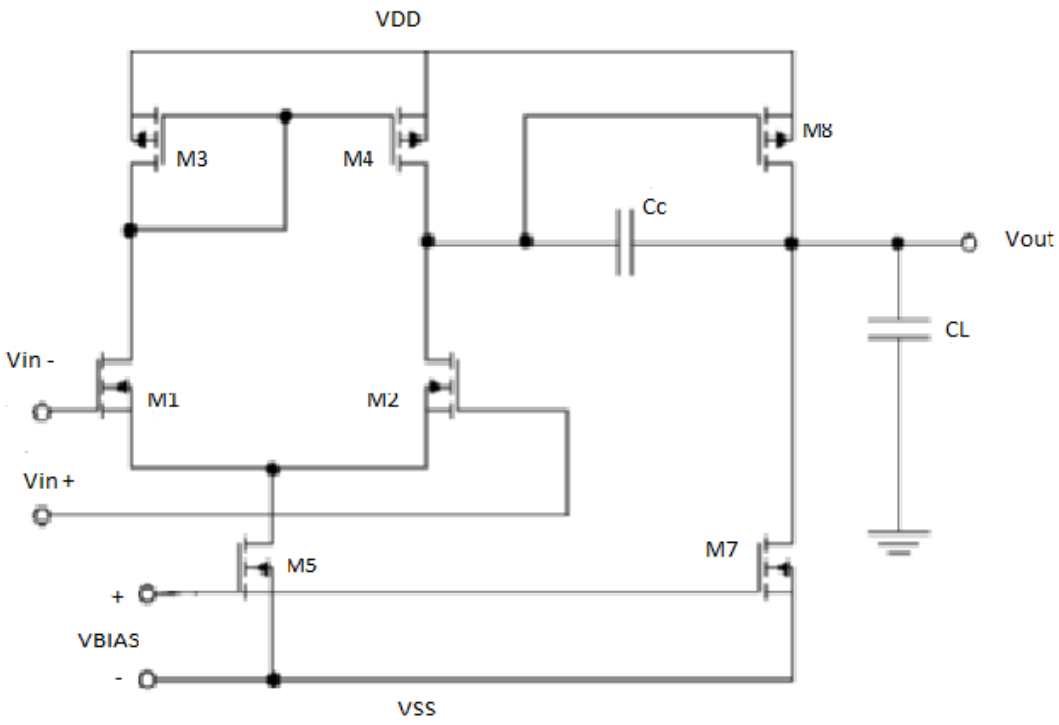

Figure 2.3 : Classical Two-stage Op-Amp [6]

2.1.2 Two Stage Op-Amp Circuit Review2 [9]

M.Idzdihar Idris, Norbayah Yusop and Siti Amaniah Mohd Chachuli proposed two Stage Op-Amp design with tittle "Low Power Operational Amplifier" in 0.13µm Technology. According to the authors, this paper is to design a low power operational amplifier consistory of two stages and operates at 1.8V power. It designed to meet a set of provided specification such as high gain and low power consumption.

Figure 2.4 shown the design proposal by authors, the first stage is an input differential amplifier and it was design to provide very high input impedance, a large CMRR and PSRR, a low offset voltage, low noise and high gain. The second stage amplifier circuit will perform level shifting, added extra gain and single to ended

conversion. Level shifting needed to compensate for DC voltage change occurring at the input stage so that an appropriate DC bias can be assure for the following stage. The added gain used to provide gain or an additional amplification to the input stage as it is not sufficient.

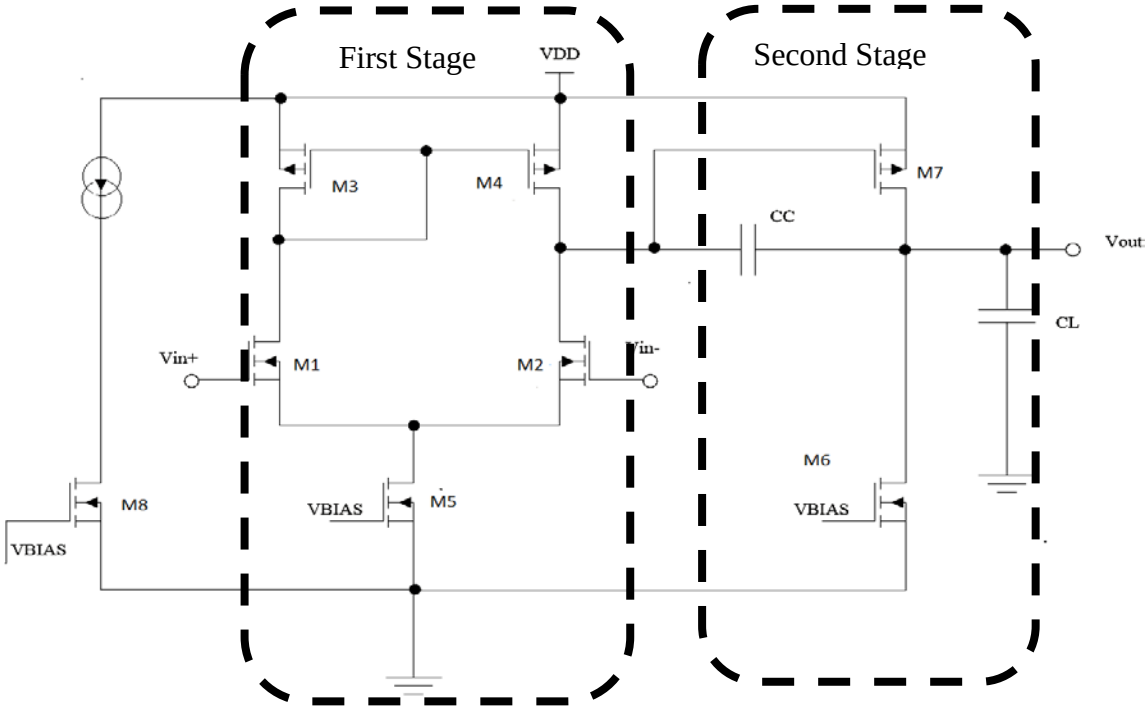

Figure 2.4: Proposed Two-stage Op-Amp Circuit Design by Authors. [9]

As before start the design, there are, several specification needs to assumed or take into consideration. The specifications are:

Table 2.1: Proposed Design Specification

Specifications	Proposed Value
Dc gain	1000/60dB
Phase margin	$\geq 60^{\circ}$
Slew rate	20V/µs
GBW	$\geq$ 30MHz
ICMR +	1.6V
ICMR -	0.8V
CL	2pF
Power dissipation	$\leq$400µW
V_{DD}	1.8V
Process	130nm

Based on the proposed schematic in Figure 2.4, the W/L ratio for M3 and M4 found from the max ICMR +, M1 and M2 is derived from the tranconductance gm1 and Gain Bandwidth (GBW). The current flow through M5 found from the slew rate. M5 and M6 is derived from minimum ICMR -, M6 from gain and the design of M3 and M4, I6 current flow to the second stage is related to the design of M3, M4 and I5, M7 is related to I5 because of the same biasing voltage and lastly the Cc value from phase margin.

The Op-Amp designed based on the given step as below:

i. The length used is 500nm.

ii. The Phase Margin specification is 60°, so he compensation capacitor equation is

$$Cc \geq 0.22\ CL \quad (2.1)$$

Where CL is load capacitance

iii. The current that flows through M5 is:

$$I5 = SR \times Cc \quad (2.2)$$

iv. Design of M1 and M2 from the gain bandwidth product (GBW) and the small signal tansconductance from gate to channel

$$gm1 = GBW \times Cc \times 2\pi \quad (2.3)$$

$$\left(\frac{W}{L}\right)_{1,2} = \frac{g_{m1^2}}{\mu_n C_{ox} \, x \, I_5} \quad (2.4)$$

v. Design of M3 and M4 is from ICMR +

$$\left(\frac{W}{L}\right)_{3,4} = \frac{I_5}{\mu_p C_{ox} \times [VDD - (ICMR_4) - Vt3_{max} + Vt1_{min}]^2} \quad (2.5)$$

vi. The transistors' size of M5 and M6 can be determined from ICMR-

$$\text{VDS5}(sat) \geq (ICMR\ -) - \sqrt{\left\{I_5 \left[\mu_n C_{ox} \left(\frac{W}{L}\right)_1\right]\right\}} - Vt1_{max} \quad (2.6)$$

$$\left(\frac{W}{L}\right)_5 = \frac{I_5}{\mu_n C_{ox} \times [\text{VDS5}(sat)]^2} \quad (2.7)$$

vii. The transistor's size of M7 from gain and related to M3 and

$$gm_6 > 10 \times gm_1 \quad (2.8)$$

$$\left(\frac{W}{L}\right)_7 = \frac{gm_6}{gm_4}\left(\frac{W}{L}\right)_4 \quad (2.9)$$

viii. Design of M8 from the design of M3 and M4

$$I_6 = \frac{\left(\frac{W}{L}\right)_{6 \text{ x } I4}}{\left(\frac{W}{L}\right)_4} \quad (2.10)$$

$$\left(\frac{W}{L}\right)_7 = (I_7 \times I_5) \times \left(\frac{W}{L}\right)_5 \quad (2.11)$$

Base on authors, the results show that the circuit is able to work at 1.8V power supply voltage (VDD) and provides gain of 69.73dB and 28.406MHz of gain bandwidth

product for a load of 2pF capacitor. Therefore, the power dissipation and the consistency of this operational amplifier are better than previously reported operational amplifier.

2.2 Bandgap Reference Circuit Review

This section presents of the bandgap voltage reference circuit's paper review from different authors.

2.2.1 Bandgap Design Review 1 [3]

The paper of "A Lower Sub-1 V CMOS Voltage Reference "was published by Sameer Somvanshi and Santhosh Kasavajjala. The bandgap design proposed by the authors was using MOSEFT in linear region and subthreshold region to regenerate PTAT and CTAT voltage to replace the resistor and BJT.

Figure 2.5 shows the proposed BGR circuit by authors. Transistor M9 act as "start-up" circuit while transistor M1, M2, M3 and M4 designed to work in saturation region and used for high power supply rejection. Transistor M5 and M6 are designed to operate a work in triode region, both transistors behave like voltage controlled resistor; the function of these two transistors is to maintain current across two branches in the circuit. Transistor M7 and M8 are designed to operate in subthreshold region where they behave as BJTs of traditional BGR which produces CTAT voltage in subthreshold region. While PTAT voltage produced by transistor M5 and M6.

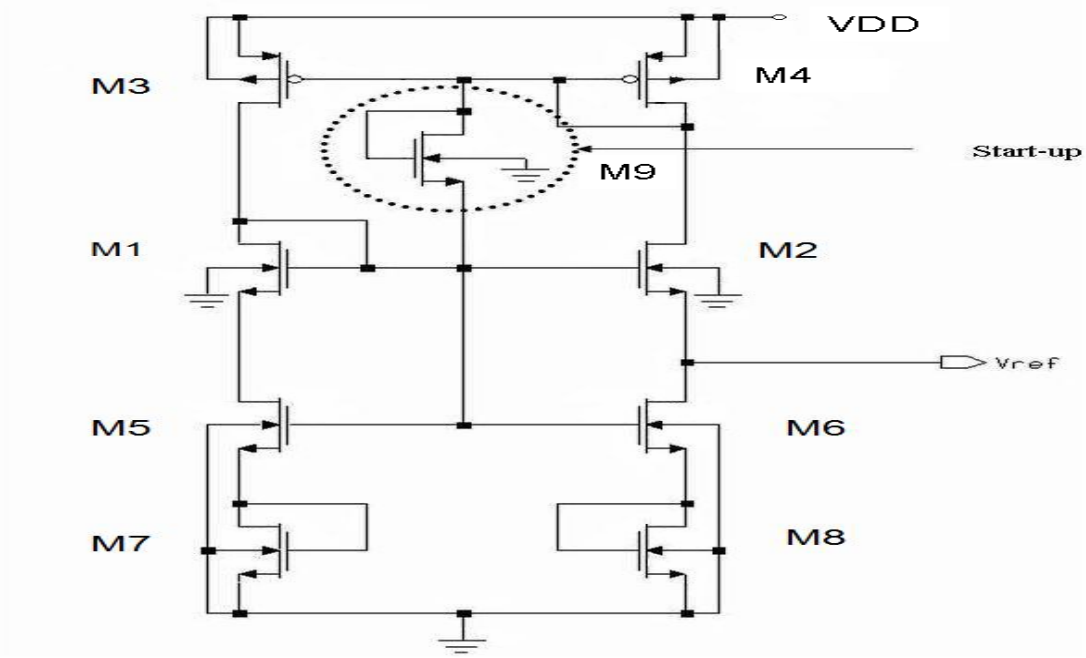

Figure 2.5: Proposed Bandgap Reference Circuit [3].

The simulation result showed, the circuit generates a stable voltage of 466.5 mV for 1.8 V power supply in 0.18 μm technologies. The temperature coefficient of circuit is 28.4 ppm/℃ in the range of -20 to +120℃. The power supply rejection measured at -30 dB at 8 KHz and low power consumption of 3.98 μW is an important attribute of this circuit.

2.2.2 Bandgap Design Review 2 [10]

Bandgap Voltage Reference with only MOS Transistors was proposed by Antonio Ribeiro, Ricardo Gama, Tiago Costa, Rui. According to the authors, the goal of the paper is to design a BGR architecture without use of an Op-Amp and using only one type of transistors and without use of parasitic BJT. The proposed of bandgap works with 1.8V supply voltage with ±10% variation in Xfab 0.18μm process. The circuit

generates an output reference voltage of 605.865 mV with a variation of ±3.325 mV over a temperature range from -40 to 85ºC, which corresponds to 1.097% variation.

The proposed bandgap voltage reference's architecture presented in Figure 2.6. The objective of the design is to only use one type of transistors in the BGR circuit that without using any Op-Amp and start-up circuit. Therefore, eight transistors make up the circuit and two resistors as shown in the Figure 2.4, transistors M1-M3 are current mirrors, M4-M5 force A node voltage to be equal to the B node voltage, in order to stabilize the circuit behavior with corner and VDD variation. Resistors R1 and R2 implement the temperature compensation. Transistors M6 and M7 produce the circuit current and make possible to transistor the M8 to be stable and preserve the voltage with VDD variation.

The output voltage given by:

$$Vref = VGSM8 + R2 \times I \approx \frac{R2}{R1} \tag{2.12}$$

The variation of V_{ref} is 6.65 mV, with minimum of 602.54 mV and the maximum of 609.19 mV. This bandgap should be used in voice applications due to circuit noise, which is 4.4 μV rms, to reduce the circuit noise the size of the transistors should be increased. The bandgap PSR is 22.5 dB at 35 kHz. One way to increase the PSR is to use an external capacitor. The proposed bandgap error is in the middle values. However, the proposed BGR only uses one type of technology, pure MOS transistors. With this, the process fabrication reduced to one type of transistors. The circuit does not use amp-op and capacitor, which can reduce the overall circuit area.

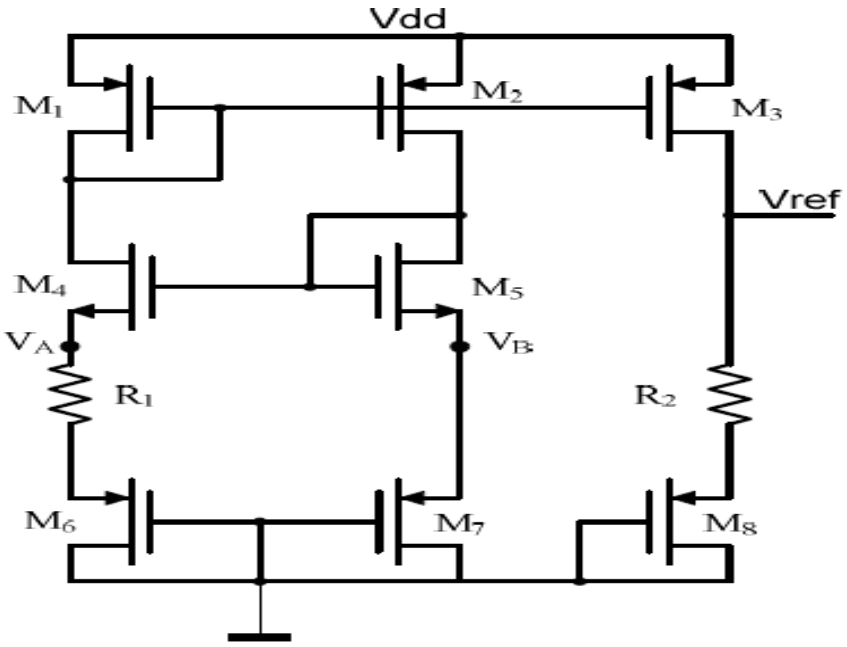

Figure 2.6: Proposed BGR Architecture [10]

2.2.3 Bandgap Design Review 3 [11]

This paper published by Chao Feng, Jin Hui Wang, Wei Wu, Ligang Hou and Jianbo Kang in 2013. The authors proposed a BGR circuit with a startup circuit by using conventional BGR bandgap Voltage Reference design. In this paper, a typical bandgap voltage reference based on CSMC 0.35 μm CMOS technology designed and fabricated. The test results show that the bandgap reference circuit provides a reference voltage of 1.2128 V to 1.2175 V with 3.3 V power supply and temperature range from -40℃ to 80℃ simultaneously, and the temperature coefficient is 32.2ppm/℃. The total layout area, including dummy structures is 135 μm×236 μm.

Figure 2.7 shows the structured of a bandgap voltage, which is composed of three different components, the startup circuit, PTAT circuit generation and CTAT, circuit generation. The startup circuit built up by M4 to M9. According to the authors, the

startup circuit is necessary to drive the circuit to work. It used to initialize the bandgap reference circuit when the power supply turned on. PTAT circuit is made up of transistors of M1 to M2 and amplifier A1, resistor R2, and BJT transistor of Q1 and Q2; the used of Op-Amp is to guarantee that node X and node Y have some current between these two branched. The PTAT current generation created by the different voltage across Q1 and Q2. The CTAT circuit formed by transistor M3, resistor R2, and BJT transistor of Q3. In proposing circuit the Voltage Base Emitter (V_{BE}), Q3 has the positive TC and the difference ΔV_{BE} between with low temperature coefficient can easily obtained by optimizing temperature-independent circuit parameters R1/R2.

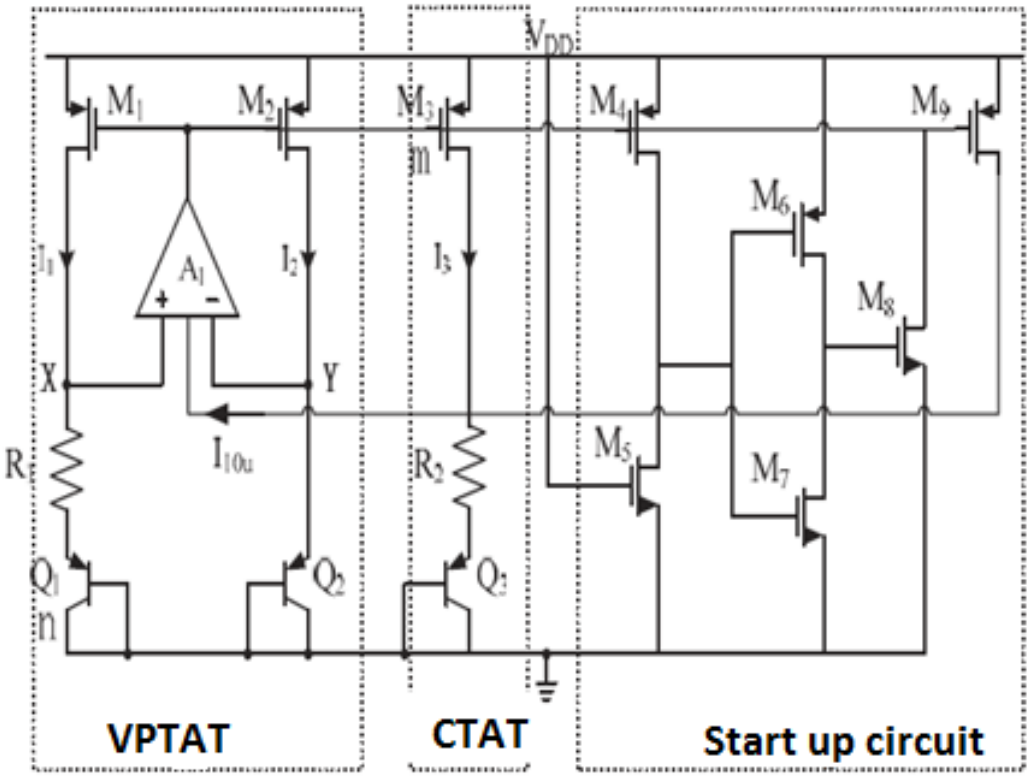

Figure 2.7: Schematic of the proposed CMOS voltage reference [11]

The bandgap reference circuit provides a reference voltage of 1.2128 V to 1.2166 V with 3.3 V power supply and temperature range over -40℃ to 80℃. The temperature coefficient is 28.6ppm/℃. While the test results show that the range of reference voltage is 1.2128 V to 1.2175 V, and the temperature coefficient is 32.2 ppm/℃ in the same temperature range as simulation set. According to authors, the fabricated circuit achieves very high accuracy of the voltage reference over wide temperature variation range.

2.2.4 Bandgap Design Review 4 [12]

LinHai Cui publishes a journal called “Design of a High Precision Bandgap Voltage Reference”. The paper proposed a high precision bandgap voltage reference by improved conventional bandgap reference circuit. The proposed circuit shown in Figure 2.8. The bandgap design built up of three parts: the startup circuit, operational amplifiers and the reference generating circuit. A PMOS active current mirror used as the load to achieve differential input, single output, which increases the speed of the circuit. The static current is limited by adjusting the function of the circuit. Meanwhile, the start current of PTAT which is proportional to temperature flows into the Op-Amp, and makes temperature compensation to let the static working point of the Op-Amp more stable.

The simulation has done by using TSMC.ll technology library. The simulation conditions are: temperature range of -40 to 140 degrees centigrade, simulation models are TT, SS, FS, SF, FF, and the precision is about 13.5 ppm/°C. Based on the authors,

the circuit are generated similar voltage reference with different powered supply setting between 1V to 1.3V at TT (typical) model simulation.

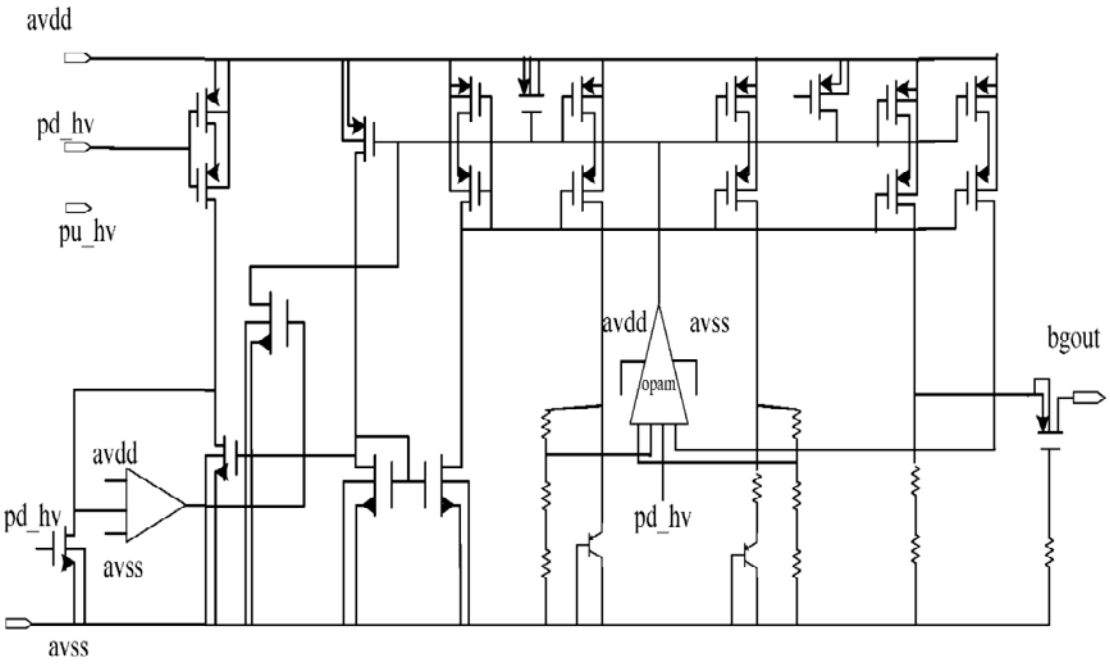

Figure 2.8: Schematic of the proposed the entire bandgap reference circuit. [12]

2.2.5 Bandgap Design Review 5 [13]

In the paper of "A Resistor less Voltage Reference Source for 90nm CMOS Technology with Low Sensitivity to Process and Temperature Variations ", A new voltage reference generator proposed by the authors is based on the well-known circuit by using MOSFET as shown in Figure 2.9. The circuit using current mirror topology is formed by transistor M1, M2, M3 and M4 by ensuring that current I1=I2.Transistor M5 and M6 are using to replace by resistance , which generated IPTAT that will flow to output load which M7 and M8 together with I9 which generated a negative temperature coefficient.

The simulation result show that the designed circuit are able to generated constant voltage of 423mV at supply voltages from 1.1V to 3.3V with total current consumption 270nA. The proposed circuit occupies 0.001 mm^2 chip area and achieves less than 110 ppm/°C for all process corners and temperature variation from -40 °C to 125 °C. Power supply rejection ratio without any filtering capacitor at 100 Hz and 10 MHz is lower than -50 dB and -30 dB, respectively.

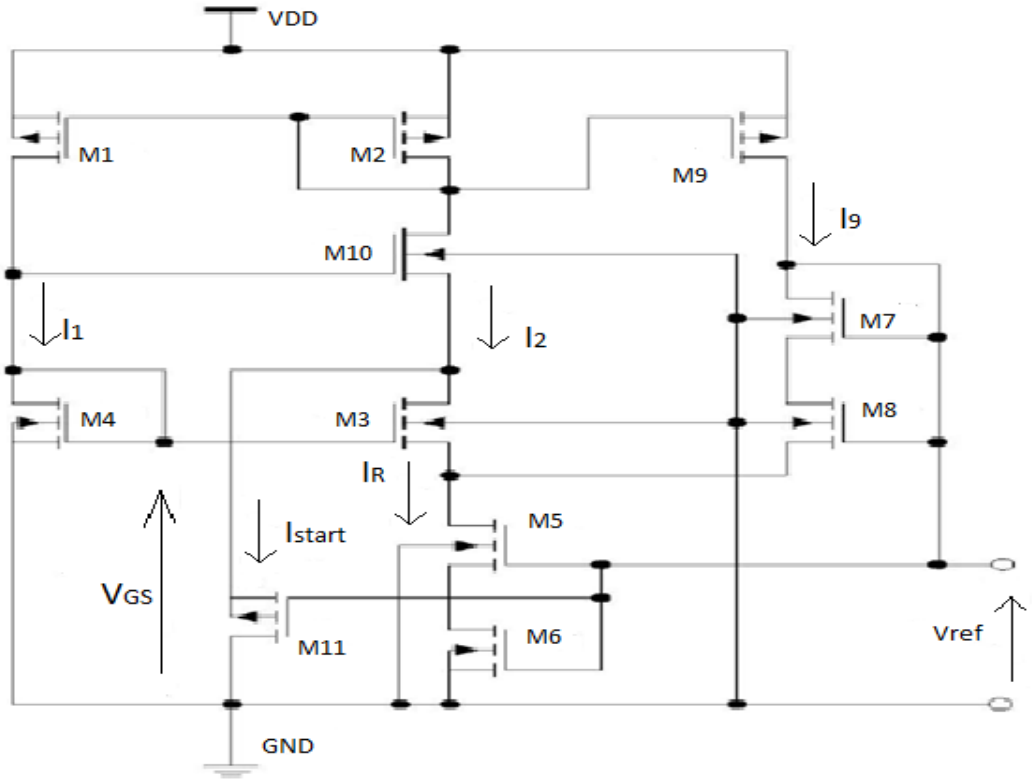

Figure 2.9: Schematic of the Bandgap Reference and Current Reference Generator [13]

2.2.6 Bandgap Design Review 6 [14]

In the paper of “Design of Bandgap Reference and Current Reference Generator with Low Supply Voltage “, the authors proposed, a precise linear CMOS bandgap voltage reference by using a resistive subdivision method which is a temperature compensated reference current generator was designed by bandgap reference voltage. The voltage reference has designed and optimized for low supply voltage and wide temperature range.

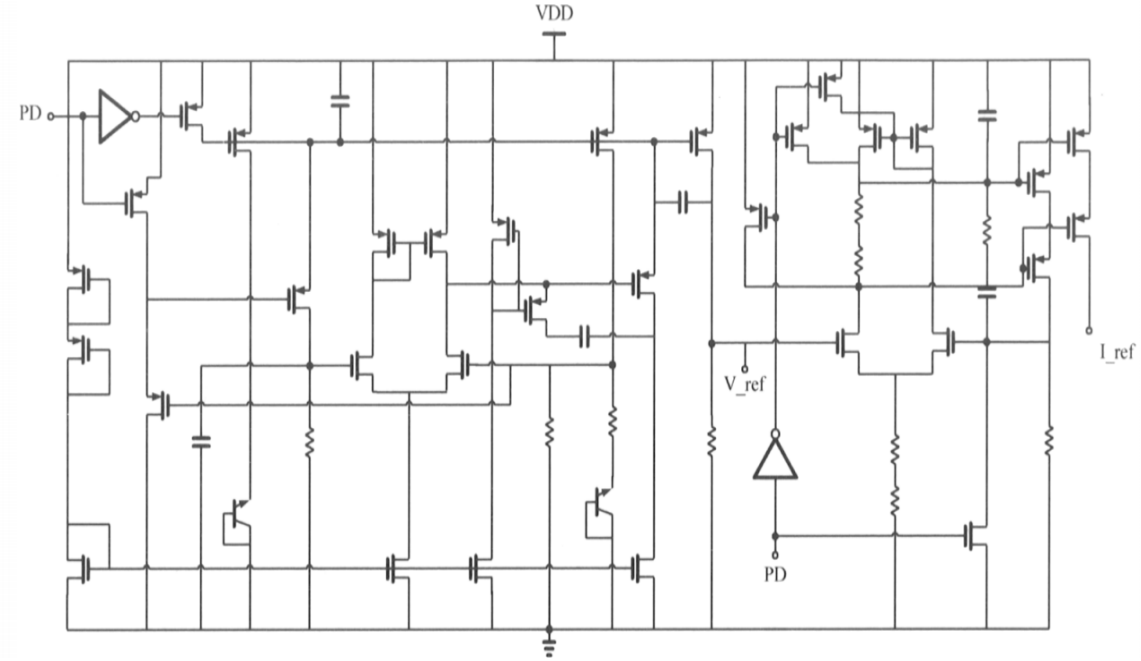

Figure 2.10: Schematic of the bandgap reference and current reference generator [14].

Figure 2.10 is the BGR design that proposed by the authors. There are total two-circuit implementation in the overall circuit: Low supply bandgap reference and current generator circuit. According to the author the output voltage of the BGR can be freely chosen by adjusting the resistor ratio, and be a more suitable voltage for low supply operation. While in the current generator circuit, the reference current generator was not

used combination of PTAT and IPTAT but generated the reference current with the bandgap reference voltage.

The circuit is able to generate an output voltage of 630mV and temperature coefficient of bandgap reference is 29ppm/°C from -10°C to 100°C with 1.2V supply voltage.

2.2.7 Summary of the Bandgap Design Review

Table 2.1 summary of the BGR design by different authors, this including the technology, temperature range, voltage supply, and temperature coefficient (TC) and power dissipation. The main feature observed in those BGR designs is voltage reference variation and the technology employed. Different authors have different kind of BGR design topology , some of them use BJT, CMOS process with parasitic BJT or BiCMOS or purely MOS transistor design , as BGR circuits are very sensitive to temperature and voltage supply variations, these are the two characteristics more focused by the authors.

Table 2.2: Summary of Different Design of BGR Circuit

Reference	[3]	[10]	[11]	[12]	[13]	[14]
Technology	0.18μm	Xfab 0.18μm	CSMC 0.35μm	TSMC.11	90nm CMOS	0.13μm CMOS
Temperature Range (℃)	-20 - 120	-40 - 85	-40 - 80	-40 - 140	-40 - 125	-10 - 110
Supply Voltage , V	1.8	1.8	3.3	1.1-1.3	1.1-3.3	1.2
Temperature Coefficient (ppm/℃)	28.4	-	32.2	13.5	110	29
Power Dissipation	3.98uW	-	-	-	891nW	-
Voltage Reference	446.5mV	605.87 mV	1.2128 V to 1.2175 V	603.3mV	423mV	630mV
Variation	1.86mV	6.65mV	5mV	1.4mV	5mV	1 mV

2.2.8 Summary

This chapter described in details the design review for second stage Op-Amp and different BGR circuit design. As due to different application, different kind of BGR circuit are able to be use as long as the circuit able to provide a constant reference voltage with independence to temperature change.

Chapter 3

METHODOLOGY

3.0 Introduction

In this chapter, present a comprehensive design flow of the BGR circuit shown as in Figure 3.1 and the simulations of the circuits are complete in Cadence Virtuoso Analog Design Environment with Silterra 0.18μm library.

After the Literature Review, the two stages of amplifier was chosen to be a part of the BGR design as it will provide high gain and phase margin for BGR circuit. Once the amplifier circuit are functioning as expected, which is the circuit are able to achieved more than 60dB gain with phase margin more than or equal to 60° , it has then been integrated into the BGR circuit.

Next, to design a BGR circuit by using conventional BGR circuit and substituting the BJT transistor by MOS transistor. The graph of V_{ref} versus Temperature is plotted to verify the functionality of BGR circuit, which able to achieve in temperature range of -10℃ to 100℃ and it operating voltage supply are 1.8V to 3.3V. If the design specs not met, some tuning on the resistor's value as well as transistors' size is needed. After the BGR circuit are functioning as expected, several simulations such as V_{ref} versus Voltage Supply (VDD) and Power Supply Rejection Ratio (PSRR) versus Frequency graph as well as Corner and Monte Carlo analysis were carry to analyze the performance of BGR circuit. Finally, the Temperature Coefficient (TC) computed based on the values obtained from the graphs plotted to evaluate the BGR to versus temperature change.